Physics AT QUEENS COLLEGE

Colloquium Notice

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Non-contact Electrical Characterization/Metrology of Advanced Gate Dielectrics and their Interface with Silicon

The non-contact, quasi-static technique presented involves biasing the silicon wafer with the gate dielectric by depositing charge (from a corona source) and measuring the surface voltage and surface photovoltage (via illumination) using a Kelvin Probe.

The main parameters of measurement presented are: Equivalent Oxide Thickness (EOT), Leakage Current, Flatband Voltage, Density of Interface Traps (D_{it}) and Soft Breakdown Field. EOT and D_{it} measurements were chosen for the metrology of gate dielectrics for manufacturing application. Density of Interface Traps, in particular, is an important parameter for qualification of the interface between the dielectric and the semiconductor. D_{it} is very sensitive to interface roughness, presence of intrinsic defects or extrinsic impurities all of which can be attributed to particular technique of the growth of the dielectric, silicon implantation specifics, annealing details etc. Examples of gate dielectrics from recent IBM/Infineon Logic and DRAM technologies will be presented.

Note: This talk is based on the work by the author while at IBM Research Division.

Wednesday
March 10, 2004
Starts at 12:15 PM
Coffee at 12:00 PM
Physics Conference Room, SB B326